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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/723,289	11/25/2003	Peter Beer	INF 2070-US	5566

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EXAMINER	
PHUNG, ANH K	

ART UNIT	PAPER NUMBER
2824	

DATE MAILED: 06/01/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/723,289	BEER, PETER	
	Examiner	Art Unit	
	ANH PHUNG	2824	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *13 May 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-16* is/are pending in the application.

4a) Of the above claim(s) *11-16* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-10* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *11/25/03*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Response to Arguments/Remarks

1. In response to the Election received on May 13, 2005, the examiner agrees with Applicant that claim **1** is generic.

The elected claims **1-10** are present for examination.

The non-elected claims **11-16** are withdrawn from further consideration.

Information Disclosure Statement

2. This office acknowledges receipt of the following items from the Applicant:

Information Disclosure Statement (IDS), filed on November 25, 2003.

Information disclosed and list on PTO 1449 was considered.

Priority

3. Receipt is acknowledged of papers submitted under 35 U.S.C. 119(a)-(d), which papers have been placed of record in the file.

Specification

Abstract

4. The abstract of the disclosure is objected to because the phraseology such as "**The invention**" was used. Correction is required. See MPEP § 608.01(b).

Applicant's cooperation is requested in correcting any errors of which applicant may become aware in the specification.

Claim Rejections - 35 USC § 102

5. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

6. Claims **1-10** are rejected under 35 U.S.C. 102(b) as being anticipated by Henkels (US 5,571,743).

Regarding independent claim 1, Henkels et al. disclose a dynamic memory cell as shown in Figures 1-10, comprising a storage capacitor (12, Figs. 1-3); a first selection transistor (T1, Fig. 3); and a second selection transistor (T2, Fig. 3); wherein depending on a selection signal (WL1, Fig. 6), a first electrode of the storage capacitor is connected to a first bit line (BL1, Fig. 6) via the first selection transistor and a second electrode of the storage capacitor is connected to a second bit line (BL2, Fig. 6) via the second selection transistor.

Regarding dependent claim 2, Henkels et al. disclose the storage capacitor (12, Figs. 1-3), the first selection transistor (T1, Fig. 3) and the second selection transistor (T2, Fig. 3) are disposed between the bit lines (BL & /BL, Fig. 3) at a location where the bit lines are parallel to one another.

Regarding dependent claim 3, Henkels et al. disclose the storage capacitor (12, Fig. 1), the first selection transistor (24, Fig. 1) and the second selection transistor (26, Fig. 1) are disposed on a substrate (14, Fig. 2a) and wherein the first and second selection transistors are in a vertically stacked (Fig. 1 & column 5, lines 41-50) arrangement relative to the storage capacitor.

Regarding dependent claim 4, Henkels et al. disclose in Figure 3, as known in the electrical art when transistor T1 is ON, there would be a current flowing from the

source of T1 (the source that connects to Cs as disclosed in column 4, lines 24-30) to the drain of T1 (the one that is connected to BL (first BL), see column 4, lines 24-30), then there is a charge applying to the BL (first BL). Also, when T2 is ON, then a charge would be applied to /BL that is the second bit line.

Regarding dependent claim 5, Henkels et al. disclose the storage capacitor (12, Figs. 1-3) comprises an inner region defining the first electrode (16, Fig. 2a), an outer region (18, Fig. 2a) defining the second electrode and an insulation layer disposed between the regions to electrically isolate the regions from one another; wherein the first selection transistor (T1, Fig. 3) is connected to the inner region (16, Fig. 2a) and the second selection transistor (T2, Fig. 3) is connected to the outer region (18, Fig. 2a), so that, in the event of the selection transistors being activated, a charge of the inner region is applied to the first bit line (BL, Fig. 3) and a charge of the outer region is applied to the second bit line (/BL, Fig. 3). (It is noted that, when T1 and T2 are ON, then the charges would be transferred to the first bit line and second bit line due to currents flowing from source to drain of these transistors.)

Regarding dependent claim 6, Henkels et al. disclose the first and second selection transistors are vertically disposed on either side of the storage capacitor (see Fig. 2c).

Regarding independent claim 7, Henkels et al. disclose a DRAM circuit, comprising a pair of bit lines comprising a first bit line (BL, Fig. 3) and a second bit line (/BL, Fig. 3); a plurality of dynamic memory cells (10, Figs. 1, 3, 6 & 7) coupled between the pair of bit lines, each dynamic memory cell comprising a storage capacitor (12 or

Cs, Figs. 1, 2a, 2c, 3, 6 & 7) for storing a charge representative of a bit value; a first selection transistor (T1, Fig. 3) coupled to a first electrode of the storage capacitor; and a second selection transistor (T2, Fig. 3) coupled to a second electrode of the storage capacitor; wherein the first and second selection transistors are vertically disposed on either side of the storage capacitor (see Fig. 2c) and wherein, depending on a selection signal (WL, Fig. 3), the first electrode of the storage capacitor is connected to the first bit line (BL, Fig. 3) via the first selection transistor (T1, Fig. 3) and the second electrode of the storage capacitor is connected to the second bit line via the second selection transistor (T2, Fig. 3), so that, in the event of the selection transistors being activated, a charge of the first electrode is applied to the first bit line and a charge of the second electrode is applied to the second bit line (It is noted that, when T1 and T2 are ON, then the charges would be transferred to the first bit line and second bit line due to currents flowing from source to drain of these transistors.); and a word line (WL, Fig. 3) coupled to the selection transistors and configured to drive the selection transistors.

Regarding dependent claim 8, Henkels et al. disclose a sense amplifier (46, Figs. 3, 6 & 7) coupled to the pair of bit lines (BL & /BL, Fig. 3, 6 & 7).

Regarding dependent claim 9, Henkels et al. disclose in Figures. 3, 6 & 7, wherein the storage capacitor, the first selection transistor and the second selection transistor of each dynamic memory cell (Cs, Figs. 3, 6 & 7) are disposed between the bit lines at a location where the bit lines are parallel to one another (BL & /BL are parallel to one another, Figs. 3, 6 & 7).

Claim Rejections - 35 USC § 103

7. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

8. Claim **10** is rejected under 35 U.S.C. 103(a) as being unpatentable over Henkels et al. (US 5,571,743) in view of Min et al. (US 6,034,879).

Regarding dependent claim 10, Henkels et al. teach a dynamic memory cell having all the basic limitations of the claimed invention as described above, except for the bit lines cross over each other at least once along their respective lengths.

Min et al. disclose in Figures 2-3, a dynamic memory cell comprising a pair of bit lines cross over each other at least once along their respective lengths.

Henkels et al. and Min et al. are common subject matter for the dynamic memory cell. Therefore, it would have been obvious for one of ordinary skill in the art at the time the invention was made to incorporated Henkels et al.'s dynamic memory cell into Min et al.'s dynamic memory device for the purpose of reducing impact of coupling noise.

Conclusion

9. The prior art made of record and not relied upon is considered pertinent to applicants disclosure.

Henkels et al. (US 5,363,327) disclose two transistor one capacitor trench DRAM cell similar to that of the present application.

Hokenmaier et al. (US 6,570,794) disclose twisted bit-line similar to that of the present application.

A shortened statutory period for response to this action is set to expire 3 (three) months and 0 (zero) day from the date of this letter. Failure to respond within the period for response will cause the application to become abandoned (see MPEP 710.02 (b)).

10. Any inquiry concerning this communication or earlier communications from the examiner should be directed to **ANH PHUNG** whose telephone number is **(571) 272-1883**. The examiner can normally be reached on Monday-Friday from 8:00 AM to 4:30 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, **RICHARD ELMS**, can be reached on **(571) 272-1869**. The fax phone number for the organization where this application or proceeding is assigned is **(703) 872-9306**.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at **866-217-9197** (toll-free).

Art Unit: 2824

AKP

Anh Phung

ANH PHUNG
PRIMARY EXAMINER